REMARKS

Claims 1-4, 6 and 7 are rejected under 35 U.S.C. 102(b), as anticipated by Hayashi et al. US Pat.
5   No.5768184. Claim 5 is objected to as being dependent upon a rejected base claim.

1. **Rejection of claims 1-4, 6 and 7 under 35 U.S.C. 102(b):**
10   Claims 1-4, 6 and 7 are rejected under 35 U.S.C. 102(b), for reasons of record that can be found on page 2 in the Office action identified above, which is part of paper no.1203.

15 **Response:**
Claim 1 is amended to form the amended claim 1 by including the limitations set forth in claim 3 and claim 5, which is allowable in this Office action. No new matter is introduced. The amended claim 1 of the present
20 application is repeated below for reference:

"1. A method for reading a non-volatile memory with multi-level output currents comprising:
providing a memory cell having a source, a drain,
25 a channel formed between the source and the drain, a first isolation layer formed on the channel, a **non-conducting dielectric layer comprising silicon nitride formed on the first isolation layer,** a second isolation layer formed on the non-conducting dielectric
30 layer and a conductor formed on the second isolation layer;
applying a first reading voltage on the conductor

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of the memory cell;

applying a second reading voltage on the drain of the memory cell; and

grounding the source of the memory cell, thereby
5 obtaining an output current;

wherein the memory cell comprises a first programming state, a second programming state, a third programming state, or a fourth programming state, and the output current comprises a maximum output current
10 corresponding to the memory cell in the first programming state, a first output current corresponding to the memory cell in the second programming state, a second output current corresponding to the memory cell in the third programming state, or a third output
15 current corresponding to the memory cell in the fourth programming state."

As described in the amended claim 1 and Fig.1 of the present application, a memory cell 10 comprises
20 a non-conducting dielectric layer 22 composed of silicon nitride, and further, at least four kinds of programming states can be obtained by injecting electrons into a first region 22a or a second region 22b of the non-conducting dielectric layer 22. That is,
25 four kinds of programming states can be obtained through varying positions and quantities of electrons in the non-conducting dielectric layer 22 in the present application.

30   However, Hayashi et al. disclose that a multi-level memory cell 2 comprises a floating gate 10 composed of polycrystalline silicon (Fig.5, & col.6, lines 4-5).

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Further, Hayashi et al. disclose that <u>four kinds of</u> <u>programming states can be obtained through varying</u> <u>quantities of electrons in the floating gate 10</u> (col.5, lines 33-47). Since Hayashi et al. neither disclose

5   a memory cell comprising a non-conducting dielectric layer composed of silicon nitride nor disclose to obtain four kinds of programming states through varying quantities and positions of electrons in the non-conducting dielectric layer, the amended claim 1

10 is patentably distinguishable from Hayashi et al. Reconsideration of the rejection over claim 1 is hereby requested.

    Additionally, claims 2-4, 6 and 7 are dependent on

15 the amended claim 1 and should be allowed if the amended claim 1 is allowed. Reconsideration of the rejection over claims 2-4, 6 and 7 is hereby requested.
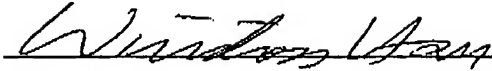

    2.Objection over claim 5:

20 Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
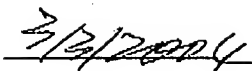

25 **Response:**
    Claim 5 is merged into the amended claim 1 and is therefore canceled. Accordingly, all claims in the present application, namely, claims 1-4 and 6-7 are now in condition for allowance. Early and

30 favorable indication of allowance is courteously solicited.

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Sincerely,

5　~~Winston Hsu~~　　　　　　　　Date: 3/2/2004

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